Simulation of an All-Optical 1×2 SMZ Switch with a High Contrast Ratio

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\textbf{ABSTRACT}
A 1×2 high contrast ratio (CR) all-optical switch based on the symmetric Mach-Zehnder (SMZ) interferometers is presented. Simulation results show a remarkable improvement of the inter-output CR (~25 dB) between the two outputs compared with an existing SMZ switch. We have shown that the proposed optical switch offers over 35 dB of inter-output CR over a wide range of input powers using appropriate power of the control pulses. The proposed switch can also support broadcast and drop switching modes when using together with an additional XOR gate.

\textbf{Keywords}
Optical switch, symmetric Mach-Zehnder, optical logic gate, high contrast ratio, broadcast mode.

\section{1. INTRODUCTION}
Optical fibre communication system has become the backbone of today’s Internet technology due to the huge transmission capacity that it offers. In packet switched optical networks, switching is still carried out in the slow electrical domain requiring optical/electrical/optical (O/E/O) conversion [1], thus, limiting the speed of the network to around 40 Gbit/s based on the current technologies [2]. Future development in electronic devices will push the speed to 80 Gbits/s or more in the next few years, thus delaying the introduction of all-optical networks. In [3, 4] it is shown that packet processing and switching can be carried out in the optical domain, hence eliminating the need for O/E/O in the main backbone super highway optical layer. For all-optical switching and routing there are a number of technologies including the terahertz optical asymmetric demultiplexer (TOAD) [5] and the symmetric Mach-Zehnder (SMZ) [6] that might be adopted because of their ultrafast switching time (pico-to-subpicoseconds) [3, 7]. Among the all-optical switches, the SMZ based switches offer a narrow symmetrical square switching window, a compact size, thermal stability, lower power operation and the greatest flexibility [8]. The SMZ function is based on the cross-phase modulation of the semiconductor optical amplifiers (SOAs) [9], where switching is performed by introducing a phase shift of 180° between the signals propagating in two arms of the interferometer [6] by injecting a high power optical control pulse to the SOAs.
However, in practice, it is a challenge to maintain an exact phase shift of 180° in SOAs. Therefore, in most cases, only the output port 1 of the SMZs are used (i.e. op1 in Fig. 1) for switching purpose due to its low inter-output CR [10]. A practical all-optical 1×2 router employing SMZs should have a high inter-output CR and lower values of output crosstalk (CXT). In this paper, we propose a novel all-optical 1×2 switch with a high inter-output CR (> 32 dB) based on three SMZs. The paper is organized as follows: after introduction, the operation principles of the SMZ, the all-optical inverter and XOR gate based on SMZ are outlined in Section 2. Section 3 introduces the proposed 1×2 switch with an additional XOR gate to support four switching modes (output 1, output 2, broadcast, and drop). Section 4 presents the simulation results and discussions. Finally, Section 5 will conclude the paper.

2. ALL-OPTICAL LOGIC GATES BASED ON SMZ

2.1 Symmetric Mach-Zehnder

Fig. 1 shows the structure of a SMZ switch comprised of SOAs and a number of 3-dB couplers. Injecting two high-power control pulses (CP1 and CP2) with a delay of $T_{SW}$ to the SOA1 and SOA2, respectively, induces the phase difference between the two arms. Thus creating a switching window (SW), and enabling the SMZ either to be switched ON or OFF. Without CPs, the upper and lower arms are in the balance state and the input signal emerges from the op2. Applying CP1 changes the gain characteristics of SOA1, and as a result the SMZ becomes un-balanced (i.e. phase difference between two arms) and the input signal emerges from the op1. With the injection of delayed CP2 to the SOA2, the SMZ is once again in the balanced state (OFF) and the input signal emerges from the op2. In order to differentiate the data pulses from the CPs at the output ports, orthogonal polarisation is introduced between the two using two polarisation controllers (PC) at the input ports followed by two polarisation beam splitters (PBS) at the output ports. The output power at the op1 and op2 of SMZ are given in [11].

The inter-output CR ($CR_{ij}$) of a 1×2 switch is defined as the power ratio between the switched and non-switched signals outputs where $i, j = 1$ or 2. Typically the value of inter-output CR observed at the SMZ output 2 ($CR_{21}$) is less than 10 dB [10]. Here we have proposed a 1×2 switch utilizing an optical inverter that offers improved $CR_{21}$.

2.2 Optical Inverter Based on SMZ

![Figure 1. A block diagram of an SMZ switch](image-url)
Fig. 2 illustrates the VPI model of an all-optical inverter [12] based on the SMZ with only op1 being (see Fig. 1) used. The input clock (CLK) signal is split and applied to the both arm of the SMZ and is also used as the control pulse CP_1 for the SOA 1. With CP_2 (i.e. CP in Fig. 4) applied to SOA 2, the SMZ is in the balanced state, thus no signal emerges from the output (\(\overline{CP}\)). With no CP_2 the SMZ becomes unbalanced, and the input signal emerges from the output port. Note that, to achieve a balanced state in the SMZ there should be no delay between CP_1 (CLK) and CP_2 and both must have the same pulse shape with equal energy. The synchronisation between CP & CLK can be achieved only when one of the input packet bit (usually use one of the header bit, depending on different applications) is extracted and then applied as a CP.

### 2.3 Optical XOR Gate Based on SMZ
Similarly, XOR logic operation can be realised by the same operation principle as in section 2.2. Here the clock signal (CLK) is applied to both arms of the SMZ and the signals A and B are used as the CPs, see Fig. 3. The output signal is high only when the SMZ is in an unbalance state (i.e. \( A \neq B \)).

3. OPERATION PRINCIPLE

3.1 1x2 High Contrast Ratio Switch Based on SMZs

Fig. 4(a) shows a schematic block diagram of the proposed 1x2 switch. Input packets are applied to the SMZ_1, SMZ_2 and to the clock extraction module (CEM) [13]. The extracted clock signal is used as the input signal as well as and the CP in the optical inverter. To achieve a high inter-output CR, only output port 1 of the SMZs are utilized with the output port 2 grounded. In the absence of CP, the input packet is switched to the output 2 since SMZ_1 is in the OFF state. When CP is high the SMZ_1 is ON and SMZ_2 is OFF, thus the packet is switched to the output 1. Synchronisation between the extracted clock signal and the CPs is essential to ensure correct operation of the switch. Fig. 4(b) shows the block diagram of the Virtual Photonics™ (VPI) equivalent of Fig. 4(a). The performances of the proposed switch will be discussed in Section 4.1.
3.2 1×2 High Contrast Ratio Switch Based on SMZs With Four Switching Modes

The features of the proposed all-optical 1×2 switch could be enhanced to support four switching modes (output 1, output 2, broadcast, and drop) using an additional optical XOR gate. Fig 5(a) illustrates the design flow of the logic circuit, CP and B (broadcast) are used as the two input signals of the logic circuit, X is the output signal applied to the SMZ1 to set its ON/OFF state. When the broadcast signal is active (B = 1), the output of the logic circuit is identical to the state of CP (i.e. X = CP), and when the broadcast signal is inactive (B = 0), the output of the logic circuit is identical to the state of \( \overline{CP} \) (i.e. \( X = \overline{CP} \)). As a result, the desired logic circuit could be implemented by having a cascaded optical inverter and optical XOR gate, which is shown in Fig. 5(b). Fig. 6(a) depicts a schematic diagram of proposed 1×2 switch with the enhanced broadcast switching capability. Here, the input packet is also applied to the SMZ1, SMZ2 and to the CEM. The extracted clock signal is having passed through a splitter is used as the input and a CP in the optical inverter and also the input in the optical XOR gate, respectively, see Figs. 2 and 3. Following the NOT operation, the output of the inverter \( \overline{CP} \) and the broadcast signal B are applied to the XOR gate. The output of the XOR gate X is then applied to SMZ2 to control its ON/OFF state. Fig. 6(b) shows the VPI equivalent of Fig. 6(a). The proposed 1×2 switch with the enhanced capability offers four different switching modes: switch the input packets to output 1, output 2, both two ports (i.e. broadcast mode), and neither port (i.e. drop mode) when \((CP, B) = (1, 0), (0, 0), (1, 1)\), and \((0, 1)\), respectively. The four different switching modes will be demonstrated in Section 4.2.

### 4. SIMULATION RESULTS AND DISCUSSION

#### 4.1 High Contrast Ratio

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inject current</td>
<td>0.15 A</td>
</tr>
<tr>
<td>Length</td>
<td>500×10^{-6} m</td>
</tr>
<tr>
<td>Width</td>
<td>3×10^{-6} m</td>
</tr>
<tr>
<td>Height</td>
<td>80×10^{-3} m</td>
</tr>
<tr>
<td>Confinement factor</td>
<td>0.15</td>
</tr>
<tr>
<td>Differential gain</td>
<td>2.78×10^{-30} m²</td>
</tr>
<tr>
<td>Carrier density at transparency</td>
<td>1.4×10^{24} m⁻³</td>
</tr>
<tr>
<td>Initial carrier density</td>
<td>3×10^{24} m⁻³</td>
</tr>
<tr>
<td>Linewidth enhancement factor</td>
<td>5</td>
</tr>
<tr>
<td>Recombine constant A</td>
<td>1.43×10⁸ s⁻¹</td>
</tr>
<tr>
<td>Recombine constant B</td>
<td>1×10⁻¹⁶ m³ s⁻¹</td>
</tr>
<tr>
<td>Recombine constant C</td>
<td>3×10⁻¹⁴ m³ s⁻¹</td>
</tr>
</tbody>
</table>

Table 1. SOA simulation parameters [14]

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data packet bit rate ( R_b = 1/T_b )</td>
<td>160 Gb/s</td>
</tr>
<tr>
<td>Bit duration ( T_b )</td>
<td>6.25 ps</td>
</tr>
<tr>
<td>Packet payload length</td>
<td>1 byte ( 8 bits)</td>
</tr>
<tr>
<td>Packet guard time</td>
<td>1.5 ns</td>
</tr>
<tr>
<td>Wavelength of data packet</td>
<td>1554 nm</td>
</tr>
<tr>
<td>Data &amp; control pulse widths (FWHM)</td>
<td>2 ps</td>
</tr>
<tr>
<td>Packet pulse peak power/energy</td>
<td>3 mW/6.81 fJ</td>
</tr>
<tr>
<td>Control pulse (CP) power/energy</td>
<td>40 mW/90.91 fJ</td>
</tr>
<tr>
<td>Broadcast signal (B) power/energy</td>
<td>14 mW/31.82 fJ</td>
</tr>
</tbody>
</table>

Table 2. Signal and control pulses default parameters

The proposed all-optical 1×2 switch is simulated using the Virtual Photonics™ (VPI) simulation software and its inter-output \( CR \) is numerically investigated. All the main simulation parameters used are shown in Tables 1 and 2. The input packet is composed of one clock bit and eight payload bits. Fig. 7(a) illustrates the captured simulated time waveforms at various points. It is shown that with CP the input packets are switched to the output 1. Fig. 7(b) shows the output power intensities (in dB) at the outputs 1 and 2, \( \overline{CP} \), and SMZ1_op1. It is observed that at the SMZ_op2, \( CR_{op1} \) of a single SMZ is about 7.5 dB (which is low). This is due to the phase shift not being exactly 180° in the SOA, thus leading to
Figure 5. (a) The design flow of the logic circuit, and (b) the logic circuit

When $B = 0$
$$X = CP$$

When $B = 1$
$$X = CP$$

<table>
<thead>
<tr>
<th>CP</th>
<th>$\overline{CP}$</th>
<th>B</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>1</td>
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</table>

Figure 6. (a) An all-optical 1×2 switch with four switching modes, and (b) VPI based model
(a)
Figure 7. (a) Output waveforms (also see the enlarged pulse waveforms), and (b) CR ratio observed at $\bar{CF}$, the proposed 1×2 switch output 1, output 2, and SMZ1_op2
Figure 8. The observed contrast ratio (CR) against (a) the input packet power and (b) the control pulse power.

Incomplete destructive signals at the SMZ_op2. By employing an optical inverter and dual SMZs, the CR1 has been significantly improved to about 35 dB. Fig. 8(a) and (b) show the inter-output CR against the input power and the control pulse power, respectively for CR, output 1 (i.e. CR1) and output 2 (i.e. CR2). The proposed 1×2 switch displays a high inter-output CR over a wide range of input powers. However, the CR is more sensitivity to the control pulse power reaching
Figure 9. Output waveforms (also see the enlarged pulse waveforms) of (a) CP, (b) CP (the output of the optical inverter), (c) B, (d) X (the output of the optical XOR gate), (e) the output 1, and (f) the output 2 of the proposed switch.

A maximum value of 35 dB at a control power of 16 dBm. Note that the CR for output 1 is almost flat compared with the others. This is because of a CP with a higher CR is applied directly to the SMZ1. The variation in the CR observed at the output 2 (i.e. CR22) is due to the CP having different power level (i.e. varying CR values) applied to the SMZ2. The obtained result indicates that the inter-output CR of the 1×2 switch is mainly dependent on the CR of the optical inverter. Note that, input signals with long PRBS sequence may cause operation failure in the current scheme due to the switching window of SMZ is not long enough compared to the packet duration of the long PRBS sequence. Additional all-optical flip-flops are required to open a long switching window for the SMZs. As a result, for long PRBS sequence switching, the complexity of the proposed switching will be increasing significantly. By employing the SOA with recovery time of 500 ps [15], the limitation of the length of the PRBS sequence is ~ 80 bits (as the packet bit duration is equal to 6.25 ps).

4.2 Four Switching Modes

Fig. 9 illustrates the captured simulated time waveforms of (a) CP, (b) CP (the output of the optical inverter), (c) B, (d) X (the output of the optical XOR gate), (e) the output 1, and (f) the output 2 of the proposed switch. From Figs. 9(b)-(d), it is shown that X is the output of the XOR operation between
CP and B. The input packets are switched to output 1 and output 2 when CP and X are non zero, respectively. This is because signals CP and X are applied to SMZ, and SMZ2 to control its ON/OFF state, see Figs. 9(a), (d), (e), and (f). The input packets are switched to output 1, output 2, both ports (i.e. broadcast mode), and neither port (i.e. drop mode) when (CP, B) = (1, 0), (0, 0), (1, 1), and (0, 1), respectively.

5. CONCLUSION
The paper has proposed and simulated an all-optical 1×2 high contrast ratio switch based on the SMZs. By appropriately setting the power of the control pulses, a high inter-output CR (> 32 dB) have been achieved over a wide dynamic range of input packet power (12 dB). The proposed 1×2 switch also offers an improvement in the inter-output CR of ~ 25 dB when compared to a single SMZ switch. We have also shown that adding an optical XOR gate to the proposed switch will facilitate four switching modes: switching to output 1, output 2, broadcasting, and dropping. With a relatively low switching time the proposed switch could potentially be adopted for high-speed signal processing and packet routing in all-optical networks.

REFERENCES

Biographies

**Dr. Ming-Feng, Chiang** received his B.S. degree in Electronic Engineering at Chung Yuan Christian University, Taiwan in 2001 and his M.S. degree in Microelectronic & Communication Engineering at Northumbria University, UK in 2005. From 2005, he joined Optical Communication Research Group at Northumbria University and received the Ph.D degree in 2009. His research interests involve All-Optical Routing & Buffering Schemes, Photonic Signal Processing, RoF, and WDM-PON. He is currently working at Information & Communications Research Laboratories, Industrial Technology Research Institute (ITRI), Taiwan.

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**Dr. Wai Pang Ng** is a Senior Lecturer at Northumbria University, United Kingdom since 2004. He received his BEng (Hons) Communication and Electronic Engineering and IEE Prize from Northumbria University in 1997. Then he pursued his graduate study, in collaboration with BT Labs and completed his PhD in Electronic Engineering at University of Wales, Swansea in 2001. Dr. Ng started his career as a Senior Networking Software Engineer at Intel Corporation from 2001 to 2004. At Northumbria University, he has published over 40 journals and conferences publications in the area of optical switching and optical signal processing. In 2005, he became Chartered Engineer of EC UK and he was elevated to Senior Member of IEEE in 2008. Dr. Ng currently serves as the vice-chair of IEEE UK&R Communication Chapter where he was also the secretary from 2007-2008. He was also the co-chair of the Signal Processing for Communications Symposium in IEEE International Conference on Communications (ICC) 2009 (Dresden, Germany).

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Mr. Ahmed Abd El Aziz received his BSc degree in Electronics and Communications from the Arab Academy for Science and Technology (AAST), Alexandria, Egypt 2003. He received his MSc degree from in Electronics and Communications specified in Optical Communications from the same University in 2006. From 2007, he achieved a studentship to start his PhD in Photonic Switching and joined Optical Communication Research Group at Northumbria University, UK. He is a teaching assistant in AAST, Alexandria, Egypt. His research interests involve Optical Communications, Optical Networks, Photonic signal processing and Photonic switching.