A Voltage Controlled Oscillator for use within a Pulse Frequency Modulation System

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Abstract

A fully integrated voltage controlled oscillator (VCO) for use within a pulse frequency modulation (PFM) system is described that achieves a linear voltage to frequency transfer characteristic over 17MHz. The output of the VCO is a pulse waveform with a duty cycle below 20 percent. The VCO is based on two grounded capacitors and is implemented in a 2.4μm CMOS technology. Due to positive feedback, no start-up conditions for the oscillator are required.

Introduction

With the development of fibre optic transmission systems, pulse time modulation techniques (PTM) experienced a renewal of interest in the late 70s and early 80s (1). PTM can be used to overcome problems associated with analogue and purely digital implementations. In PTM, the modulated carrier has a constant amplitude but variable pulse edge, width, position, or frequency. Since the form of the signal is similar to a binary pulse pattern, the received signal is not affected by channel non-linearities and has the advantage that it can be routed through logic circuitry (2). For transmission of video, audio, and data signals over optical fibre cable two PTM methods, squarewave frequency modulation (SWFM) and pulse frequency modulation (PFM), have been adopted because of their relatively superior performance compared to other PTM techniques (3).

SWFM and PFM are closely related to FM. In SWFM a square wave is used as carrier compared to a sine wave as in FM. PFM can be generated from SWFM by differentiating the SWFM signal using standard logic circuits. PFM is an attractive scheme for transmitting information using semiconductor laser diodes (LD). This is due to its low duty cycle ratio, thus allowing a high peak power with a low average power.

Both, SWFM and PFM signals can easily be generated using a voltage controlled oscillator (VCO). A block diagram of a PFM transmitter is shown in Figure 1. It basically consists of two inputs one for video the other for audio signals. The audio signal is frequency modulated onto a 6MHz carrier. Both, video and audio signals are added and the resulting signal is used as input into the VCO. The output of the VCO is the SWFM waveform. A pulse shaping circuit is used to convert the SWFM signal into the required PFM signal.

![Figure 1: Overall system block diagram](image)

Voltage controlled oscillator

The VCO is the key element of the PFM system. Two main relaxation VCO topologies can be distinguished, the floating and the grounded capacitor VCO. The first type of oscillator is mostly implemented as emitter coupled multivibrator (4).

The second type of relaxation oscillator relies on charging and discharging of a grounded capacitor. An outline of the circuit is shown in Figure 2.

![Figure 2: VCO based on grounded capacitor](image)
The capacitor $C_t$ is alternatively charged and discharged at a constant current $I_c$. The operation of the circuit is easily understood and well described in (4). If the switching delay is not considered, the frequency of oscillation is related to the control voltage $V_{in}$ as follows:

$$f_o = \frac{1}{T} = \frac{I_c (V_{in})}{2(V_{th} - V_{tl}) C_t}$$  

(1)

where $V_{th}$ and $V_{tl}$ are the upper and lower threshold voltages of the Schmitt trigger, respectively.

This circuit suffers from several disadvantages (5). Since the capacitor is charged and discharged at a constant current, two different types of voltage-controlled current sources have to be designed, one which will be an NMOS type and a second which will be PMOS type. In practice, it will be very difficult to obtain the same current characteristic for both types of sources. Furthermore, this circuit is not well suited for low voltage applications since the two reference voltages $V_{th}$ and $V_{tl}$ have to be separated from the supply voltage thus limiting the total amplitude across $C_t$, resulting in increased cycle to cycle jitter (6). Switching of the output signal will occur at two different threshold voltages resulting in problems achieving a fifty percent duty cycle.

Banu (7) proposed a VCO circuit which employs two grounded capacitors which are charged with a non-constant current and discharged over a voltage controlled current source with a lower but constant current resulting in quicker charging than discharging. Only the controlled discharging of the timing capacitor is used as frequency determining cycle. Flynn and Lidholm (5) used that principle for a voltage controlled oscillator which is optimised towards duty cycle whereas Banu’s VCO has been improved for maximum speed.

M1/M4 conducting and M2/M3 not conducting then C1 is charged with current $I_c$ and C2 is discharged over M4 with $I_d(M4)$. When the voltage across C1 reaches the threshold voltage of the double RS latch (U1-U4). M1/M4 are switched off and M2/M3 are switched on resulting in charging of C2 with the constant current $I_c$ and discharging of C1 over M2. During charging the voltage across the capacitor is:

$$V_{C1,3} = \frac{I_c}{C_{1,2}}$$  

(2)

It can be seen from Figure 3 that, with an appropriate design (M2/M4 have a higher current drive capability than M1/M3), the discharging is carried out much faster than the charging of the capacitors. Therefore, the discharging does not have any affect upon the switching point of the double RS latch. The use of a double RS latch, implemented using NAND gates, is to prevent any positive DC feedback which may freeze the RS latch into a stable state (7). Flynn and Lidholm proposed a different circuit in which the RS latch is based on a double-differential latching comparator (5) with the intention to improve, among other things, the duty cycle. The improvement of the duty cycle is achieved with lower operating speed due to higher complexity of the circuit. Both circuits have been simulated. Using an RS latch based on NAND gates resulted in excellent speed but a fifty percent duty cycle could not be achieved. This is due to the fact that different types of MOSFETs are responsible for switching from low to high and high to low. Employing the double-differential latching comparator achieves an excellent fifty percent duty cycle but at a much lower speed.

A fifty percent duty cycle is only essential when dealing with SWFM signals, since any deviation away from this will result in generation of even harmonics in the output frequency spectrum. On the other hand, a PFM signal is, by definition, a pulse waveform of a very low duty cycle. Important factors for a PFM system are a linear voltage to frequency transfer characteristic over a certain range of input voltages, good high frequency performance, and low duty cycle. Due to the latter two requirements, the circuit based on NAND gates has been implemented.

**Design Implementation**

The pulse shaping of the VCO output signal is achieved using standard digital components with inverters used as delay elements. A pulse is obtained by logically combining the delayed and the original signal using an AND gate.
The output signal is the required PFM waveform with a pulse width equal to the total delay time. An output driver has to be implemented to an appropriate specification to drive any capacitive and/or resistive load.

The voltage controlled oscillator has been implemented using the MIETEC ALCATEL 2.4µm analogue CMOS technology. Figure 5 shows the silicon layout of the VCO including the pulse shaping circuitry. The size of the design is 1.7mm by 1.9mm.

The design has been implemented using the ALCATEL MIETEC 2.4µm CMOS analogue technology (double-metal, double-poly, single n-well). The timing capacitors have been designed using two polysilicon layers separated by silicon dioxide.

Single p-type MOSFETs have been used as simple voltage to current converters and standard cells were used for bonding pads. The output bonding pad has a driver circuit built in. The design itself has been implemented, apart from the bonding pads, at transistor level.

**Simulation results**

The VCO has been simulated at different input voltages to determine its linearity and highest achievable frequency. The simulations have been carried out with the parasitic capacitances but no load capacitances included. In addition, the output driver has not been considered but Wakayama and Abidi (5) have experimentally shown that a similar driver had a rise time of 2.2ns which is sufficient for this design. Measurements on a 150µm/3µm NMOS with a 8pF load capacitance have shown a fall time of 3.42ns using the Mietec Alcatel 2.4µm CMOS technology. Measured rise time for the PMOST was 6.07ns.

Figure 6 shows the PFM waveform obtained. The pulse width is about 8ns at a period of 48.2ns resulting in a duty cycle of 16.6 percent.

![PFM waveform](image-url)

**Simulation set-up**

The VCO has been designed on a HP712 workstation using Mentor Graphics (Version A1F) IC Station for silicon layout and HSPICE (Version 95) for simulation. From the silicon layout the SPICE netlist with lumped parasitic capacitances has been extracted. Distributed parasitic extraction would have been the preferred method but because of software problems within the netlist extraction tool this method could not be applied.

Figure 7 shows the result of the linearity test. The linear region reaches from 3.66MHz at \( V_{in}=1.4\,\text{V} \) to 20.75MHz at \( V_{in}=2.8\,\text{V} \) (\( V_{in}=5\,\text{V}-V_{dd} \)). Above 2.8V the frequency of the VCO seems to settle due to reduced drain-source voltage of M1 and M3 driving them into the ohmic region.
A voltage controlled oscillator which can be used in a pulse frequency modulation system has been described. Produced in a 2.4µm CMOS technology the VCO can be used to modulate video, audio, and data signals for transmission over optical fibre. The small size of the VCO allows the implementation of a whole PFM system on a single chip. The simulation results show that the device has a very good linearity over a frequency range of 4 to 21MHz. The circuit has been optimised for low duty cycle as required for driving laser diodes.

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**References**


